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Eric Link

(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

Eric Link

(SIGNATURE OF PERSON MAILING PAPER OR FEE)

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ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

Transmitted herewith for filing is the patent application of:

Inventors: **GUINEA ET AL.**

For: **A DETECTOR FOR DETECTING TIMING IN A DATA FLOW**

Enclosed are:

[X] Patent Application: 15 pages, 6 claims.

[X] 4 Sheets of drawings.

[X] A Preliminary Amendment.

[X] Citation Under 37 CFR 1.97 and PTO-1449.

[X] Submission of Proposed Drawing Modification.

The Declaration and Filing Fee are **NOT ENCLOSED.**

[X] Name, Address and Citizenship of Inventor(s) is as follows:

Jesus GUINEA
Via Arnichi, 2
24041 Brembate Bergamo Italy
Citizen of Italy

Luciano TOMASINI
Via L. Rota, 44
20052 Monza Milano, Italy
Citizen of Italy

PLEASE ADDRESS ALL CORRESPONDENCE TO ATTORNEY OF RECORD

CHRISTOPHER F. REGAN
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
P.O. Box 3791
Orlando, FL 32802-3791

Date: August 10, 2000

Michael W. Taylor

Michael W. Taylor
Reg. No. 43,182

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Eric Link

(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

Eric Link

(SIGNATURE OF PERSON MAILING PAPER OR FEE)

In re Patent Application of: **GUINEA ET AL.**

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **A DETECTOR FOR DETECTING TIMING IN A DATA FLOW**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label the blocks in FIGS. 1-2 and 5-7.

In the Specification:

Page 3, delete lines 21-23 beginning with "According to the present invention, ..." and substitute the following therefore:

-- This and other objects, features and advantages in accordance with the present invention are provided by a detector for detecting timing in a digital data flow with a predetermined bit-time, and with a coding that provides at a beginning of the bit-time no transition, or a transition of a

first type, or a transition of a second type, and provides in a middle of the bit-time no transition, or the transition of the first type.

The detector comprises a first circuit for generating four timing signals each having a period substantially equal to the bit-time. The four timing signals are out of phase with one another by 1/4 period. A second circuit samples the four timing signals upon each transition of the first type in the data flow, and determines based upon the sampling whether two of the four timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow. The second circuit also controls the first circuit to delay or advance the four timing signals based upon the pair of reference signals.

The second circuit comprises a sampling circuit, and a decoding circuit connected to the sampling circuit for decoding the sampled four timing signals. The sampling circuit preferably comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow. The decoding circuit preferably comprises a logic circuit connected to respective outputs of the four bistable elements for determining whether the pair of reference signals is advanced or delayed relative to the timing of the data flow. -

<u>In the Claims</u>:

Please cancel Claims 1-5.

Please add new Claims 6-33.

6. A detector for detecting timing in a data flow with a bit-time, and with a coding that provides at a beginning of the bit-time no transition, or a transition of a first type, or a transition of a second type, and provides in a middle of the bit-time no transition, or the transition of the first type, the detector comprising:

a first circuit for generating four local timing signals each having a period substantially equal to the bit-time, the four local timing signals being out of phase with one another by 1/4 period; and

a second circuit for sampling the four local timing signals upon each transition of the first type in the data flow, and for determining based upon sampling whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow, and for controlling said first circuit to delay or advance the four local timing signals based upon the pair of reference signals.

7. A detector according to Claim 6, wherein the coding comprises a coded mark inversion coding.

8. A detector according to Claim 6, wherein said second circuit comprises:

a sampling circuit; and

a decoding circuit connected to said sampling circuit for decoding the sampled four local timing signals, and connected to said first circuit for control thereof.

9. A detector according to Claim 8, wherein said sampling circuit comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein said decoding circuit comprises a logic circuit connected to respective outputs of said four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

10. A detector according to Claim 9, wherein each one of said bistable elements comprises a D-type flip-flop; and wherein said logic circuit comprises a pair of AND gates connected to the outputs of said four bistable elements, a NOR gate connected to respective outputs of said pair of AND gates, and an INVERTER connected to an output of said NOR gate.

11. A detector according to Claim 10, wherein a first one of said pair of AND gates is connected to two of said four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements for receiving as inputs logic complements of the remaining two timing signals.

12. A detector for detecting timing in a data flow comprising:

a first circuit for generating four local timing signals each having a period substantially equal to a bit-time of the data flow, the four local timing signals being out of phase with one another by 1/4 period; and

a second circuit for determining based upon a sampling of the four local timing signals whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow, and for controlling said first circuit to delay or advance the four local timing signals based upon the pair of reference signals.

13. A detector according to Claim 12, wherein the data flow comprises coding for providing at a beginning of the bit-time no transition, or the transition of a first type, or a transition of a second type, and providing in a middle of the bit-time no transition, or the transition of the first type.

14. A detector according to Claim 12, wherein the coding comprises a coded mark inversion coding.

15. A detector according to Claim 12, wherein said second circuit comprises:

a sampling circuit for sampling the four local timing signals upon each transition of the first type in the data flow; and

a decoding circuit connected to said sampling circuit for decoding the sampled four local timing signals.

16. A detector according to Claim 15, wherein said sampling circuit comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein said decoding circuit comprises a logic circuit connected to respective outputs of said four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

17. A detector according to Claim 16, wherein each one of said bistable elements comprises a D-type flip-flop; and wherein said logic circuit comprises a pair of AND gates connected to the outputs of said four bistable elements, a NOR gate connected to respective outputs of said pair of AND gates, and an INVERTER connected to an output of said NOR gate.

18. A detector according to Claim 16, wherein a first one of said pair of AND gates is connected to two of said four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements for receiving as inputs logic complements of the remaining two timing signals.

19. A data transmission network comprising:
a processing circuit for processing data;
a transmission medium; and

an interface circuit connected between said processing circuit and said transmission medium for interfacing a data flow therebetween, said interface circuit comprising a detector for detecting timing in the data flow, said detector comprising

a first circuit for generating four local timing signals each having a period substantially equal to a bit-time of the data flow, the four local timing signals being out of phase with one another by 1/4 period, and

a second circuit for determining based upon a sampling of the four local timing signals whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow, and for controlling said first circuit to delay or advance the four local timing signals based upon the pair of reference signals.

20. A data transmission network according to Claim 19, wherein the data flow comprises coding for providing at a beginning of the bit-time no transition, or the transition of a first type, or a transition of a second type, and providing in a middle of the bit-time no transition, or the transition of the first type.

21. A data transmission network according to Claim 20, wherein the coding comprises a coded mark inversion coding.

22. A data transmission network according to Claim 19, further comprising a remote interface circuit connected to said transmission medium for receiving the data flow from said interface unit and for transmitting the data flow to said interface circuit.

23. A data transmission network according to Claim 19, wherein said processing circuit and said interface circuit conform to a synchronous digital hierarchy standard.

24. A data transmission network according to Claim 19, wherein said second circuit comprises:

a sampling circuit for sampling the four local timing signals upon each transition of the first type in the data flow; and

a decoding circuit connected to said sampling circuit for decoding the sampled four local timing signals.

25. A data transmission network according to Claim 24, wherein said sampling circuit comprises four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein said decoding circuit comprises a logic circuit connected to respective outputs of said four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

26. A data transmission network according to Claim 25, wherein each one of said bistable elements comprises a D-

type flip-flop; and wherein said logic circuit comprises a pair of AND gates connected to the outputs of said four bistable elements, a NOR gate connected to respective outputs of said pair of AND gates, and an INVERTER connected to an output of said NOR gate.

27. A data transmission network according to Claim 26, wherein a first one of said pair of AND gates is connected to two of said four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements for receiving as inputs logic complements of the remaining two timing signals.

28. A method for detecting timing in a data flow comprising:

generating four local timing signals each having a period substantially equal to a bit-time of the data flow, the four local timing signals being out of phase with one another by 1/4 period;

sampling the four local timing signals upon each transition of a first type in the data flow;

determining based upon the sampling whether two of the four local timing signals forming a pair of reference signals that are out of phase by ½ period are advanced or delayed relative to the timing of the data flow; and

delaying or advancing the four local timing signals based upon the pair of reference signals.

29. A detector according to Claim 28, wherein the data flow comprises coding for providing at a beginning of the bit-time no transition, or the transition of the first type, or a transition of a second type, and providing in a middle of the bit-time no transition, or the transition of the first type.

30. A detector according to Claim 28, wherein the coding comprises a coded mark inversion coding.

31. A detector according to Claim 28, wherein after the sampling of the four local timing signals the method further comprises decoding the sampled four local timing signals.

32. A detector according to Claim 31, wherein the sampling is performed by a sampling circuit comprising four bistable elements, each bistable element being associated with a respective timing signal and being clocked by the transitions of the first type in the data flow; and wherein the decoding is performed using a logic circuit connected to respective outputs of the four bistable elements for determining whether the pair of reference signals are advanced or delayed relative to the timing of the data flow.

33. A detector according to Claim 32, wherein a first one of said pair of AND gates is connected to two of the four bistable elements for receiving as inputs the two of the four local timing signals forming the pair of reference signals, and a second one of said pair of AND gates is connected to a remaining two of said four bistable elements

for receiving as inputs logic complements of the remaining two timing signals.

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

Michael W. Taylor

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorney for Applicants

A DETECTOR FOR DETECTING TIMING IN A DATA FLOW

Field of the Invention

The present invention relates to the field of data-transmission networks, and more particularly, to a synchronous data transmission, particularly in accordance with a synchronous digital hierarchy (SDH) standard. More particularly, the present invention relates to a detector for detecting timing in a data flow.

Background of the Invention

The synchronous digital hierarchy (SDH) standard prescribes the following predetermined transmission rates: 51.84 Mbit/s (base rate), 155.52 Mbit/s, 622.08 Mbit/s, etc. All of the prescribed transmission rates are whole multiples of the base rate.

The G.703 recommendation issued by the CCITT committee of the International Telecommunication Union (ITU) prescribes the electrical and physical characteristics of the hierarchy digital interfaces to be used for interconnecting components of digital networks which conform to the SDH standard. In particular, recommendation G.703 prescribes the type of data coding to be used for each transmission rate. For example, for 155.52 Mbit/s transmission/receiving

interfaces, coded mark inversion (CMI) coding should be used. These interfaces are also known as bidirectional or transceiver interfaces.

CMI coding is a coding with two levels, A1 < A2, in which a binary 0 is encoded to have the two levels A1 and A2 in succession, each for a time equal to half of the bit-time. A binary 1 is encoded by one of the two levels A1, A2 which is maintained throughout the bit-time. The two levels A1, A2 are alternated for successive binary 1s. The encoded CMI signal is therefore characterized in that, in the middle of the bit-time, there are no transitions or there are transitions with leading edges. Conversely, at the beginning of the bit-time, there may be either upward or downward transitions.

In general, in data-transmission networks there is a need to synchronize a component of the network with a data flow coming from a remote unit. This need arises, for example, in interfaces which are associated with digital circuits for processing data received and/or to be transmitted and which, typically, operate on data which is encoded differently. For example, the data may be coded in accordance with non-return-to-zero (NRZ) coding.

During receiving, the interface therefore has to receive a signal containing CMI-encoded data from a remote analog interface by a transmission/receiving channel formed, for example, by a pair of coaxial cables. The interface must also recognize the data, convert it into NRZ, and supply it to the digital circuits for processing. During transmission, the interface receives NRZ-encoded data from the digital processing circuits, recognizes the data, converts it into CMI, and provides the data on the transmission/receiving channel.

Timing detectors are used for synchronizing a component of the transmission network, such as an interface of the type described above for a flow of data arriving from a remote unit, for example. Due to the characteristics of CMI coding which, as stated, also has transitions in the middle of the bit-time, known timing detectors require local clock signals with a frequency of twice the frequency of the flow of data arriving, i.e., twice the data rate, to be able to produce the two transitions within the bit-time which are typical of CMI coding. In the example of a 155.52 Mbit/s data flow corresponding to a bit-time of 6.43 ns, the local clock signals have a frequency of 311.04 MHz.

Summary of the Invention

In view of the foregoing background, it is therefore an object of the present invention to provide a detector for detecting timing in a data flow which does not require local clock signals with a frequency greater than that of the data flow itself.

According to the present invention, this object is achieved by a synchronous bidirectional interface according to Claim 1.

Brief Description of the Drawings

The characteristics and the advantages of the present invention will become clearer from the following detailed description of an embodiment thereof, illustrated purely by way of a non-limiting example in the appended drawings, in which:

Figure 1 is a block diagram of a circuit comprising a timing detector for detecting the timing in a data flow according to the present invention;

Figure 2 is a block diagram of the timing detector according to the present invention;

Figure 3 is a schematic diagram of one embodiment of the timing detector illustrated in Figure 2;

Figure 4 is a graph illustrating the operating principle of the timing detector according to the present invention;

Figure 5 is a block diagram of a data-transmission network including a timing detector according to the present invention;

Figure 6 is a block diagram of a receiving/ transmission interface included in the network illustrated in Figure 4; and

Figure 7 is a block diagram in greater detail of two functional blocks of the interface illustrated in Figure 6, one of which includes a timing detector according to the present invention.

Detailed Description of the Preferred Embodiments

With reference to Figure 1, a circuit for detecting timing in a data flow BK comprises a circuit 1 for generating a local clock signal CK. The local clock signal CK is supplied to a circuit 2 to obtain, from the signal, four local timing signals Q1, Q2, Q3, Q4 having the same period T. This period is equal or substantially equal to the bit-time of the data flow BK. The signals Q1-Q4 are out of phase with one another by T/4. The signal Q2 is delayed by T/4 relative to the signal Q1. The signal Q3 is delayed by T/4 relative to the signal Q2, and by T/2 relative to the signal Q1. That is, the signal Q3 is in quadrature relative to the signal Q1. The signal Q4 is delayed by T/4 relative to the signal Q3.

The four signals Q1-Q4 are supplied to a timing detector 3 which also receives the data flow BK, the timing of which is to be detected. The detector 3 generates a signal +/- which is supplied to the circuit 2. A first level of the signal +/- indicates to the circuit 2 that the signal Q1 is delayed relative to the timing of the data flow BK and should be advanced. Conversely, a second level of the signal +/- indicates to the circuit 2 that the signal Q1 is advanced relative to the timing of the data flow BK and should be delayed.

If the signal Q1 is advanced or delayed, the signals Q2-Q4 are also consequently advanced or delayed. Their delays relative to the signal Q1 are kept constant. Once the signal Q1 is synchronized with the timing of the data flow BK, it can be used by other circuit blocks to perform processing on the data flow BK. An example of using signal Q1 is provided below.

Figure 2 shows a block diagram of the circuit 3 of Figure 1. The timing detector comprises a sampling circuit 100 which samples the four signals Q1-Q4 in synchronization with the leading edges of the signal BK, and supplies sampled signals Q1C-Q4C to a decoding circuit 101 which decodes the states of the sampled signals Q1C-Q4C to activate the signal +/-.

An implementation of the circuit of Figure 2, which is in no way limiting, is shown in Figure 3. The circuit comprises four D-type flip-flops FF1-FF4 which receive the signals Q1-Q4 at their respective data inputs D, whereas their sampling inputs receive in common the data flow BK. A reset signal RES is also supplied to the reset inputs of the flips-flops FF1-FF4 for re-establishing certain starting conditions.

The output Q1', the negated output Q2N' of the flip-flops FF1 and FF2, the output Q3', and the

negated output Q4N' of the flip-flops FF3, FF4 are supplied to an AND-NOR-INVERTER logic gate 4. The logic complement of the output of the logic gate 4 forms the signal +/-.

The circuit of Figure 3 performs the logic function:

+/- = Q1' AND Q2N', OR Q3' AND Q4N'

After the flip-flops have been loaded with the values applied to their inputs, Q1', Q2N', Q3', Q4N' are respectively equal to Q1, Q2N, Q3, Q4N.

Since, one of the signals Q1 and Q3 and one of the signals Q2 and Q4 is always complementary to the respective other signal, the circuit of Figure 3 has the following truth table:

Q4	Q3	Q2	Q1	+/-
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

The operating principle of the above-described timing detector will now be explained with reference to the timing graph of Figure 4. The data flow BK acts as a sampling signal for the flip-flops FF1-FF4. At the leading edges of the signal BK, the logic states applied to the inputs D of the flip-flops FF1-FF4 are stored and supplied as outputs. Prior to the time instant t1, the four signals Q1-Q4 are assumed to be represented by the continuous lines. The signal Q1, which is to be synchronized with the timing of the data flow BK, is advanced by Δt.

At the leading edge of the signal BK (time instant t1) which, in the example shown, is formed by the transition in the middle of the bit-time typical of a logic 0 signal. The states of the signals are Q1 = 1, Q2 = 0, Q3 = 0, and Q4 = 1. On the basis of the truth table given above, the above-mentioned states correspond to signal +/- = 1 which indicates to the circuit 2 that the signal Q1 is advanced and should be delayed.

The circuit 2 consequently provides for the signal Q1 and, correspondingly, for the signals Q2-Q4 to be delayed. The lines with single dots in Figure 4 indicate the edges of the signals Q1-Q4 as they would be if the circuit 2 did not intervene to delay them.

At the time instant t2 corresponding to the next leading edge of the signal BK which, in the example, is again the transition in the middle of a bit-period of a logic 0 signal. The signal Q1 is still advanced relative to the data flow BK. The flip-flops FF1-FF4 sample and load the new states of the signals Q1-Q4. Since the new state coincides with the previous one, the signal +/- generated is again a 1, and the circuit 2 therefore once more provides for the signal Q1 and, consequently, for the signals Q2-Q4 to be delayed. In Figure 4, the lines with double dots indicate the edges of the signals Q1-Q4 as they would be after the first intervention of the circuit 2.

The next leading edge of the signal BK at the time instant t3, which corresponds to a logic 1 signal, is at the beginning of the bit-time. The flip-flops FF1-FF4 sample the new state of the signals Q1-Q4 which, on the basis of the truth table given above, again correspond to a logic 1 on the signal +/-. The four signals Q1-Q4 are therefore delayed again. At the instant t3, the signals Q3 and Q4 are utilized for

locking onto the transition at the beginning of the bit-time.

The signals Q1 and Q3 are thus progressively and dynamically kept in synchronization with the leading edges of the signal BK. The synchronization is both at the beginning and in the middle of the bit-time. Locking with the timing of the data flow is thus achieved. The signals Q1 and Q3 may be used by other circuit blocks for synchronizing the blocks with the timing of the data flow that is arriving. The signals Q2 and Q4 may be used by the circuit blocks to perform sampling of the data flow every half bit-time.

An advantage of the timing detector according to the present invention is that it does not require local timing signals with a frequency of twice the bit frequency of the data flow, the timing of which is to be detected. The four signals Q1-Q4, which are out of phase with one another by one quarter of the bit-time, and all of the transitions of the CMI-coded signal with leading edges may be used for synchronization. That is, both the transitions at the beginning of the bit-time (corresponding to logic 1 signals) and those in the middle of the bit-time (corresponding to logic 0 signals) may be used. For example, the signals Q1 and Q2 serve for locking with the transitions in the middle of the bit-time, and the signals Q3 and Q4 serve for locking with the transitions at the beginning of the bit-time.

Although in the example described, the four signals Q1-Q4 have duty cycles equal to 50%. The use of the four signals Q1-Q4 which are out of phase by one quarter of the bit-time also enables the timing detector to operate independently of the duty cycle of the local timing signals Q1-Q4, and to be insensitive to changes in the duty cycle of the signals Q1-Q4.

The following Figures 5-7 illustrate one possible application of the timing detector according to the present invention. Figure 5 shows schematically a data-transmission network, and in particular, a network conforming to the synchronous digital hierarchy (SDH) standard. A bidirectional, synchronous interface 5, i.e., a transmission and receiving interface, receives digital data with CMI coding from a remote far end analog interface 7 on a first channel 6a, such as a coaxial cable, for example.

The interface 5 in turn transmits a flow of digital data with CMI coding to the remote interface 7 on a second channel 6b also formed, for example, by a coaxial cable. For the interface 5, the channel 6a is the receiving channel (RX), and the channel 6b is the transmission channel (TX). The interface 5 communicates with digital circuitry 8 for processing the data received and to be transmitted. Similarly, the remote interface 7 is associated with respective digital circuitry 9.

As shown in Figure 6, the interface 5 comprises an equalizer circuit 10 for module and phase equalization of the signal received on the receiving channel RX. A signal RXEQ output from the equalizer circuit 10 with CMI coding is supplied in parallel to a circuit 11 for recovering the timing signal during receiving, and to a decoding circuit 12. The decoding circuit 12 decodes the CMI-coded signal RXEQ into a corresponding signal RXNRZ with NRZ coding, for example, that is suitable for supply to the digital circuitry 8.

The circuit 11 for recovering the timing signal during receiving also receives n timing signals CK1-CKn of equal period T, delayed relative to one another by T/n, where T is the bit-time. In the case

of a 155.52 Mbit/s synchronous receiving/transmission interface, the bit-time is about 6.43 ns. For example, there are sixteen signals CK1-CKn, with a signal CKi+1 being delayed by T/16 relative to a signal CKi. The signals CK1-CKn are generated by a delay locking circuit 13 or a delay locked loop (DLL) supplied with a clock signal CK of period T.

The clock signal CK is in turn generated by a local circuit 14 which generates a pair of differential signals TXCKA, TXCKB conforming to the low voltage differential signal levels (LVDS) which are transformed into the signal CK conforming to the CMOS levels (e.g., 3.3 V or 5 V) by an LVDS/CMOS input buffer 15. The circuit 14 may, for example, be within the digital circuitry 8 and is used to generate a pair of differential signals TXDA, TXDB representing the flow of bits to be transmitted.

The NRZ-coded signals TXDA, TXDB are transformed by the input buffer 15 into a signal DATA. This signal DATA is still NRZ-coded and is transformed by an NRZ to CMI encoding circuit 16 synchronized with a timing signal CKTX. The timing signal is generated by the digital circuitry 8, and has a frequency equal to that of the signal CK, but a duty cycle which is guaranteed to be substantially equal to 50%. A subsequent driver circuit 17 receives the signal from the encoding circuit 16 and provides the signal TX to be transmitted.

The circuit 11 for recovering the timing signal during receiving generates a recovered timing signal CKR which is supplied to the decoding circuit 12. This circuit has to be synchronized with the flow of bits received to be able to decode the CMI signal to NRZ.

The signal RXNRZ and the signal CKR are also supplied to the digital circuitry 8 after their levels have been transformed from CMOS to LVDS by a CMOS/LVDS output buffer 18. This output buffer 18 is similar to the input buffer 15, and transforms the signal RXRNZ into a pair of differential signals RXDA, RXDB and the signal CKR into a pair of differential signals RXCKA, RXCKB.

Figure 7 shows the delay locking circuit 13 and the timing-signal recovery circuit 11 in greater detail. The circuit 13 is composed of a chain of n (e.g., n = 16) delay elements T1-Tn in cascade. These delay elements are controlled by a logic unit 19 which receives an output signal 20 from a phase comparator 21. The chain of delay elements T1-Tn form a controlled delay line. The overall delay introduced by the delay line T1-Tn is controlled so that the delay is equal to one period T of the signal CK.

The phase comparator 21 receives as inputs and compares the signal CK and the signal CKn at the output of the last delay element Tn of the chain. The output signal 20 of the phase comparator 21 depends on the phase difference detected between the signals CK and Ckn. The logic unit 19 controls the delay elements T1-Tn so that the delay introduced by each of delay elements is such that the signal CKn is in phase the with signal CK, less one period T.

The outputs CK1-CKn of the n delay elements T1-Tn are supplied to a selection circuit 22. The selection circuit 22 is basically a multiplier in the recovery circuit 11. Of the n (n = 16 in the example) input signals CK1-CKn, the multiplier 22 outputs four signals Q1-Q4 delayed relative to one another by T/4. The four signals Q1-Q4 are supplied to a timing detector 23 according to the present invention.

The timing detector 23 is of the type described above, which also receives the signal RXEQ with CMI coding. The timing detector 23 controls the selector 22 by the signal +/- as described above, in a manner such that the signal Q1, which corresponds to the signal CKR that is supplied to the decoder 12, is synchronized with the data flow during receiving.

The clock signal is thus recovered from the signal received and can be supplied to the CMI to NRZ decoding circuit 12. In other words, during receiving, the interface is synchronized with the flow of data received. The interface described has the advantage of requiring only one local timing signal, i.e., a single time base, which is used both for transmission and for the recovery of the clock signal during receiving.

The timing of the interface both during receiving and during transmission is thus entrusted to a single time base. This eliminates the need to provide two local oscillators with frequencies close to one another, and hence the risk of crosstalk between the two timing signals. A saving in terms of components and power absorbed is also achieved. Variations of and/or additions to the embodiments described above and illustrated may be provided, without departing from the scope of the present invention.

THAT WHICH IS CLAIMED IS:

1. A detector for detecting timing in a digital data flow (BK) with a bit-time equal to T and with a coding which provides, at the beginning of the bit-time T, for no transition or for a transition of a first or a transition of a second type and, in the middle of the bit-time T, for no transition or for a transition of the first type characterized in that it comprises first circuit means (2) for generating four local timing signals (Q1-Q4) which have periods substantially equal to the bit-time and are out of phase with one another by 1/4 period, and second circuit means (3) for sampling the four local timing signals (Q1-Q4) upon each transition of the first type in the data flow and for determining, on the basis of the sampled states of the four local timing signals (Q1-Q4), whether a pair of reference signals (Q1-Q3) which are out of phase by one half period, of the four local timing signals (Q1-Q4), are advanced or delayed relative to the timing of the data flow, and consequently controlling the first circuit means in a manner such as to delay or to advance the four local timing signals (Q1-Q4).

2. A timing detector according to Claim 1, in which the coding is a CMI (coded mark inversion) coding.

3. A timing detector according to Claim 2, characterized in that the second circuit means (3) comprise circuit means (100; FF1-FF4) for sampling the four local timing signals (Q1-Q4) upon each transition of the first type in the data flow (BK), and circuit means (101; 4) which decode the sampled states of the

four local timing signals (Q1-Q4) and which control the first circuit means (2).

4. A detector according to Claim 3, characterized in that the sampling circuit means comprise four bistable elements (FF1-FF4) of which each is associated with a respective signal (Q1-Q4) of the four local timing signals and all are clocked by the transitions of the first type in the data flow (BK), and the decoding circuit means comprise a combinational circuit (4) which receives the outputs of the bistable elements (FF1-FF4) and which, on the basis of the states of the said outputs, determines whether the said pair of reference signals (Q1, Q3) are advanced or delayed relative to the timing of the data flow (BK) and consequently controls the first circuit means (2).

5. A timing detector according to Claim 4, characterized in that the bistable elements are D-type flip-flops and the combinational circuit (4) comprises an AND-OR-INVERT gate which receives the outputs of the flip-flips (FF1-FF4) as inputs.

6. A timing detector according to Claim 5, characterized in that the AND-OR-INVERT gate receives as inputs a pair of sampled signals (Q1', Q3') corresponding to the pair of reference signals (Q1, Q3), and a second pair of sampled signals (Q2N', Q4N') corresponding to the logic complements of the remaining two local timing signals (Q2, Q4).

A DETECTOR FOR DETECTING TIMING IN A DATA FLOW

Abstract of the Disclosure

A detector detects timing in a digital data flow with a bit-time equal to T, and with a coding that provides at a beginning of the bit-time no transition, or a transition of a first type, or a transition of a second type, and provides in a middle of the bit-time T no transition, or for the transition of the first type. A first circuit generates four local timing signals each having periods substantially equal to the bit-time. Each of the four local timing signals are out of phase with one another by 1/4 period. A second circuit samples the four local timing signals upon each transition of the first type for determining, based upon the sampling, whether two of the four local timing signals forming a pair of reference signals that are out of phase by 1/2 period are advanced or delayed relative to the timing of the data flow. The second circuit controls the first circuit for delaying or advancing the four local timing signals based upon the pair of reference signals.

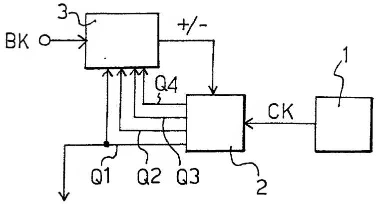


FIG.1

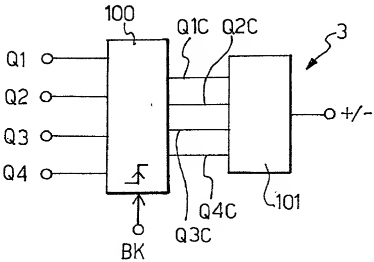


FIG.2

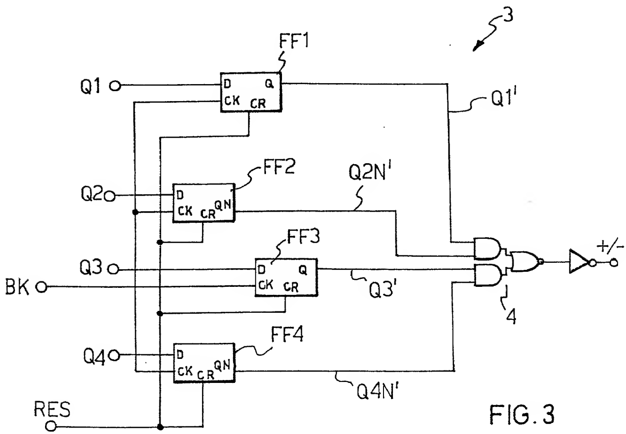


FIG.3

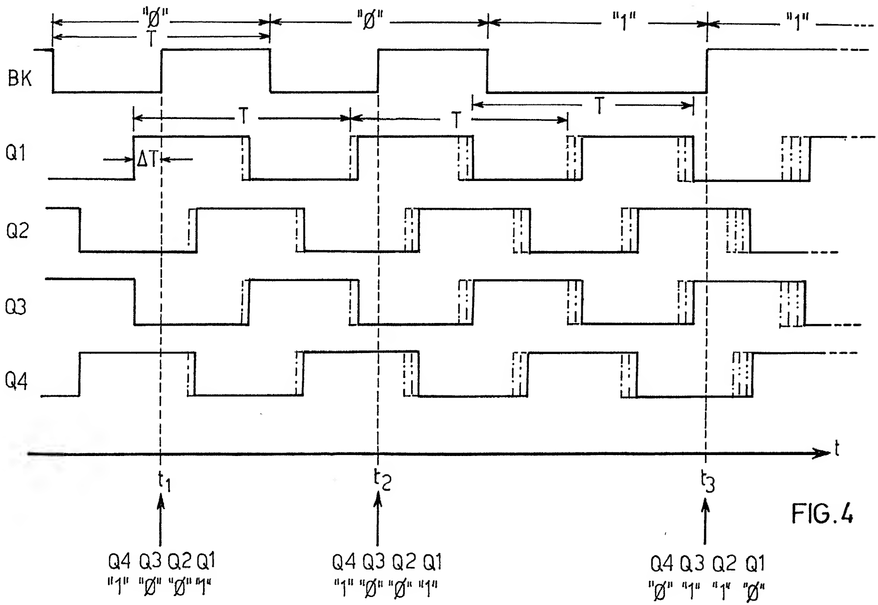

"Ø"
T
"Ø"
"1"
"1"
BK
T
T
T
Q1
ΔT
Q2
Q3
Q4
t
t1
t2
t3
Q4 Q3 Q2 Q1
"1" "Ø" "Ø" "1"
Q4 Q3 Q2 Q1
"1" "Ø" "Ø" "1"
Q4 Q3 Q2 Q1
"Ø" "1" "1" "Ø"

FIG.4

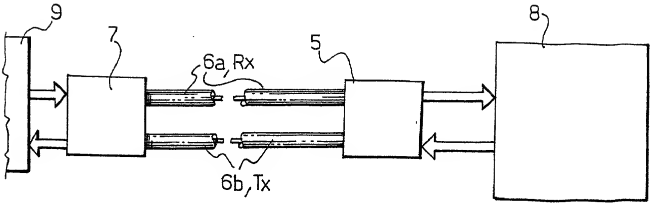

9
7
6a, Rx
5
8
6b, Tx

FIG.5

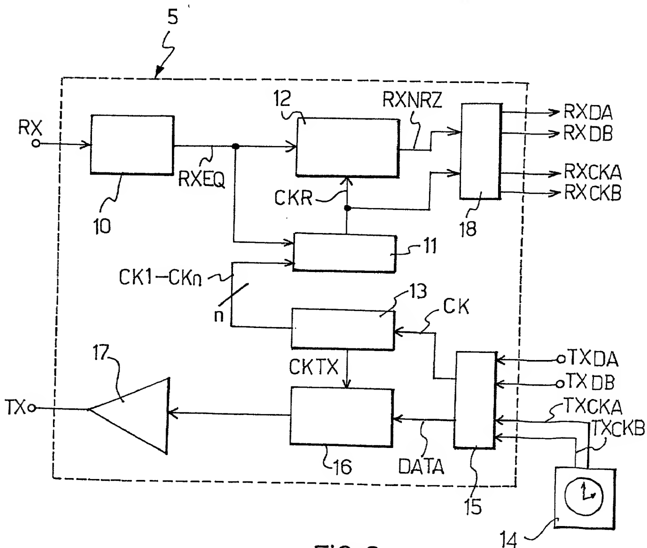

5
RX
12
RXNRZ
RXDA
RXDB
RXEQ
CKR
RXCKA
RXCKB
10
18
11
CK1—CKn
n
13
CK
17
CKTX
TXDA
TXDB
TXCKA
TXCKB
TX
16
DATA
15
14

FIG.6

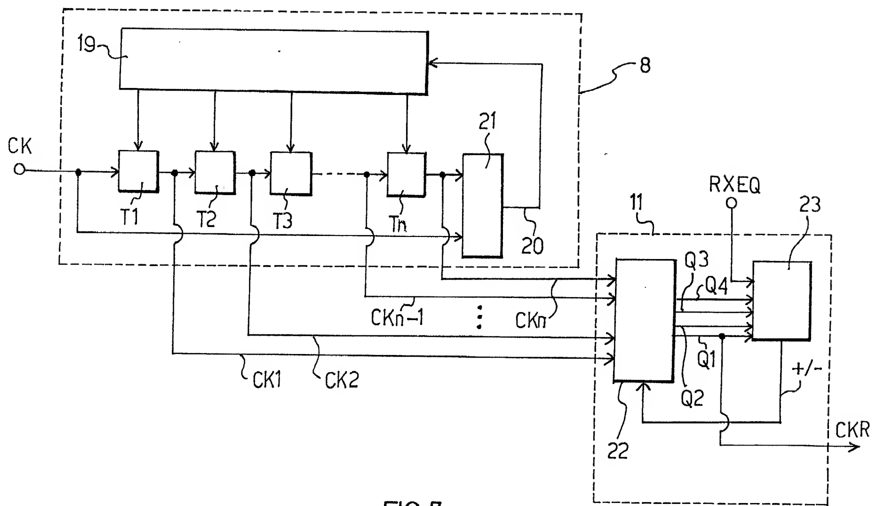

8
19
CK
T1
T2
T3
Tn
21
20
11
RXEQ
23
Q3
Q4
Q1
Q2
CKn-1
CKn
CK1
CK2
+/-
22
CKR

FIG.7

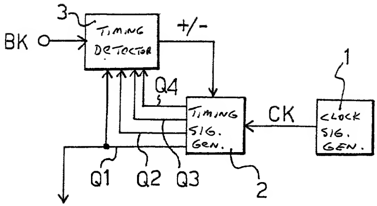


FIG.1

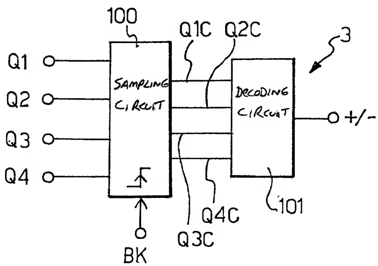


FIG.2

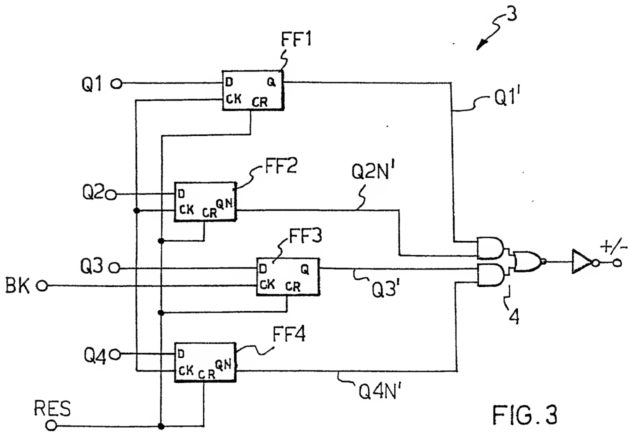


FIG.3

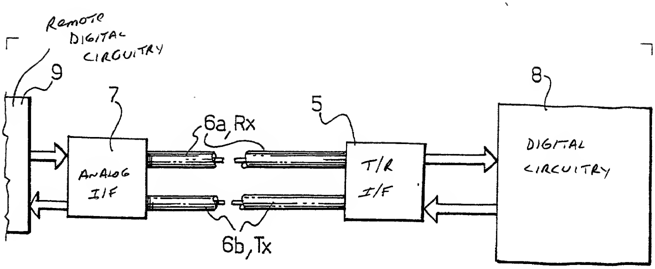

Remote DIGITAL CIRCUITRY
9
7
ANALOG I/F
6a, Rx
6b, Tx
5
T/R I/F
8
DIGITAL CIRCUITRY

FIG.5

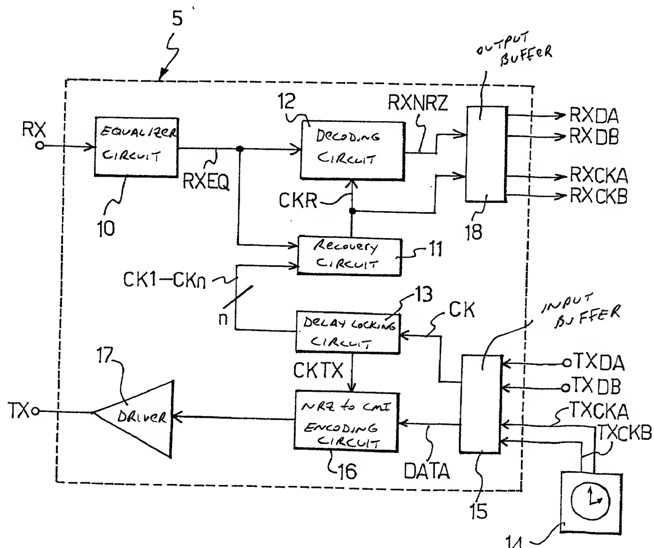
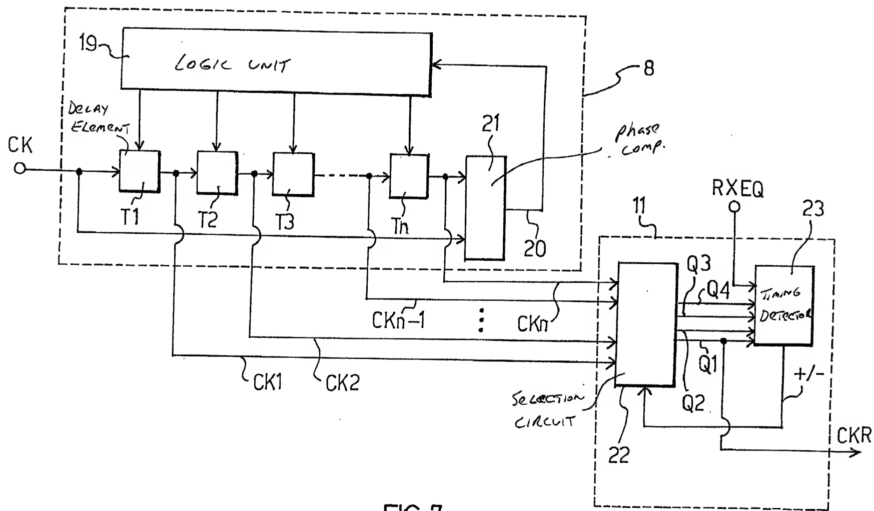

5
OUTPUT BUFFER
RX
EQUALIZER CIRCUIT
10
RXEQ
12
DECODING CIRCUIT
RXNRZ
CKR
18
RXDA
RXDB
RXCKA
RXCKB
RECOVERY CIRCUIT
11
CK1—CKn
n
13
DELAY LOCKING CIRCUIT
CK
INPUT BUFFER
CKTX
17
DRIVER
TX
NRZ to CMI ENCODING CIRCUIT
16
DATA
15
TXDA
TXDB
TXCKA
TXCKB
14

FIG.6



CK
Delay Element
19
Logic Unit
8
T1
T2
T3
Th
21
20
phase comp.
11
RXEQ
23
Q3
Q4
Timing Detector
Q1
Q2
+/-
CKn-1
CKn
CK1
CK2
Selection circuit
22
CKR

FIG.7